## CLAIMS

having thus described our invention in detail, what we claim is new and desire to secure by the letters Patent is:

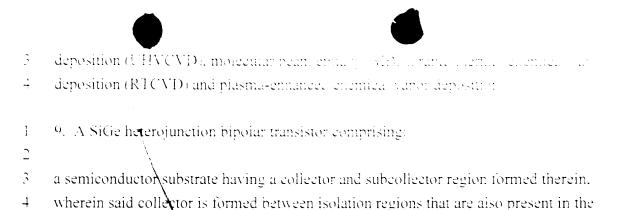
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- 1. A method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar transistor comprising the steps of:
- (a) forming a passivation layer on at least exposed sidewalls of an emitter, said emitter
- is in contact with an underlying SiGe base region through an emitter opening formed
- 6 in an insulator layer; and

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- 8 (b) siliciding expased silicon surfaces so as to form silicide regions therein.
- 1 2. The method of Claim 1 wherein said passivation layer is formed from a rapid
- 2 thermal chemical vapor deposition process.
- 1 3. The method of Claim 1 wherein said passivation layer is composed of a nitride, an
- 2 oxide, an oxynitride or any combination thereof.
- 1 4. The method of Claim 1 wherein said passivation layer is a nitride passivation layer.
- 5. The method of Claim 4 wherein said nitride passivation layer is formed from a
- 2 rapid thermal chemical vapor deposition process which is carried out in a nitrogen-
- 3 containing atmosphere.
- 6. The method of Claim 5 wherein said nitrogen-containing atmosphere is selected
- 2 from the group consisting of NO,  $N_2O$  and  $N_2$ .

- 7. The method of Claim 4 wherein said rapid thermal chemical vapor deposition process is carried out at a temperature of about 700°C or greater.
- 8. The method of Claim 1 wherein said SiGe base region is formed by a deposition
- 2 process selected from the group consisting of ultra-high vacuum chemical vapor



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substrate:

a SiGe layer formed on said substrate, said SiGe layer including polycrystalline Si regions formed above said isolation regions and a SiGe base region formed above said collector and subcollector regions:

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a patterned insulator layer formed on said SiGe base region, said patterned insulator layer having an opening therein:

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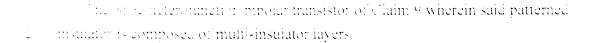
an emitter formed on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter having exposed sidewalls:

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a conformal passivation layer formed on at least said exposed sidewalls of said emitter; and

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- silicide regions formed on exposed portions of said SiGe layer and said emitter not
- 21 covered by said conformal passivation layer.
- 1 10. The SiGe heterojunction bipolar transistor of Claim 9 wherein said semiconductor
- substrate is selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP, other
- 3 III/V compound semiconductors, Si/Si and Si/SiGe.
- 1 11. The SiGe heterojunction bipolar transistor of Claim 9 wherein said emitter is
- 2 composed of intrinsic polysilicon.
- 1 12. The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned
- 2 insulator is composed of SiO<sub>2</sub> or Si oxynitride.



- 14. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation
- 2 layer is also formed on vertical sidewalls of said patterned insulator and portions of
- 3 said SiGe base region.

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- 4 15. The SiGe heterojunction bipolar transistor of Claim 9 wherein said silicide
- 5 regions are formed in an exposed horizontal surface of said emitter, said
- 6 polycrystalline Si region and a portion of said SiGe base region.
- 1 16. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation
- 2 layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.
- 1 17. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation
- 2 layer is a nitride passivation layer.

